REMARKS

Claims 1-20 were originally filed in the present application.

Claims 1, 2, 4-10 and 12-20 are pending in the present application.

Claims 1, 2, 4-10 and 12-20 were finally rejected in the July 18, 2005, Office Action.

No claims have been allowed.

No claims are amended herein

Claims 1, 2, 4-10 and 12-20 remain in the present application.

Reconsideration of the claims is respectfully requested.

In Sections 1 and 2 of the July 18, 2005, Office Action, the Examiner rejected Claims 1, 2, 9, 10, 12 and 17 under 35 U.S.C. 103(a) as being unpatentable over United States Patent No. 5,889,816 to *Agrawal et al.* (hereafter, "*Agrawal*") in view of United States Patent No. 6,282,604 to *May* (hereafter, "*May*"). In Section 3 of the November 16, 2004 Office Action, the Examiner rejected Claims 6-8, 14-16 and 18-20 as unpatentable over *Agrawal* in view of *May* in further view of United States Patent No. 5,995,831 to *Gulliford et al.* (hereafter, "*Gulliford*"). In Section 4 of the November 16, 2004 Office Action, the Examiner rejected Claims 4, 5, 12 and 13 as unpatentable over *Agrawal* in view of *O'Connell* in further view of United States Patent No. 6,308,080 to *Burt et al.* (hereafter, "*Burt*"). The Applicant respectfully traverses these rejections.

The Applicant respectfully directs the Examiner's attention to amended independent Claim 1, which contains the unique and novel limitations herein emphasized:

> 1. (Currently Amended) For use in a base station of a wireless network, a call control processor comprising:

> a first state machine capable of performing a call processing task in response to receipt of a message retrieved from an operating system queue associated with said first state machine, said first state machine comprising an internal queue capable of storing a plurality of events associated with said call processing task, each of said plurality of events operable to cause said first state machine to perform a selected action, wherein said first state machine is capable of communicating with a second state machine of said call control processor by storing at least one event directly into an internal queue associated with said second state machine.

The Applicant respectfully submits that the above-emphasized limitations are not disclosed, suggested, or even hinted at in any one of the *Agrawal*, *May*, *Gulliford*, and *Burt* references individually, or in any combination of two or more of the *Agrawal*, *May*, *Gulliford* and *Burt* references.

In the July 18, 2005, final Office Action, the Examiner acknowledges that *Agrawal* lacks a description of state machines having internal queues and a first state machine storing events directly into an internal queue of a second state machine. However, the Examiner asserted that *May* provides such a teaching in Fig. 5 and at column 6, lines 1-16, and column 11, lines 28-50. The Applicant respectfully submits that the Examiner mischaracterizes the teaching of the *May* reference.

The passage at column 6, lines 1-16, of the *May* reference states:

> A Request Queuing Finite State Machine 156 has an internal queue (not shown) for storing memory request information, including the address, operation type, and Case signal value, for each memory request received by the memory controller. It stores the information for each received request in its internal queue (not shown) and transfers them to the Packet Issuing Finite State Machine 150 when various timing and system constraints, not relevant to the present invention, have been satisfied. Each time a new memory request is received, this state machine 150 responds to storing the request, including the Case selection signal value for the request, and then asserting Write Bank State. At the next system clock cycle, the Write Bank State and system clock signal operate together to store updated bank state values in the bank state cache, as will be explained below. (*Emphasis added*)

Thus, the first cited passage discloses a first finite state machine storing requests in its own internal queue and transferring the requests to a second finite state machine.

The second cited passage, at column 11, lines 28-50, describes the logic circuitry of the Next Bank State Encoder and contains no references to finite state machines or internal queues. The succeeding paragraph of the *May* reference, at column 11, lines 51-63, teaches that the output signals of the Next Bank State Encoder are written into the Bank State Cache upon the assertion of a Write signal indicating that a memory request has been received and stored in the internal queue of the Request Queuing Finite State Machine, described in the first cited passage.

As such, the Applicant respectfully submits that the *May* reference does not, in fact, teach a first state machine communicating with a second state machine by storing an event directly into a queue associated with the second machine, as recited in independent Claim 1. Moreover, the *Gulliford* reference and the *Burt* reference fail to overcome the shortcomings of the *Agrawal* reference and the *May* reference with respect to Claim 1.

In the July 18, 2005, final Office Action, the Examiner asserted that a person of ordinary skill in the art would have modified the system of the *Agrawal* reference by the teaching of the *May* reference "in order to make data transfer as efficient as possible by using the minimum number of control packets needed to service requests," citing the *May* reference especially at column 2, lines 40-50. The cited passage states:

> Another object of the present invention is to provide a memory controller for dependent bank DRAM devices that simultaneously accesses state information for an addressed bank and state information for its neighboring banks from a cache of bank

> state information, and then utilizes that information to determine the minimum number of control packets needed to service a specified memory request.

The teaching of the cited passage is that the use of state information regarding an addressed bank and neighboring banks of DRAM devices allows a memory controller to determine the minimum number of control packets needed to service a memory request. The *Agrawal* reference, on the other hand, describes a system in which a plurality of state machines operating on a base station CPU communicate using queues managed by the operating system of the CPU. The Applicant respectfully submits that there is thus no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the wireless networking adapter of the *Agrawal* reference as taught by the memory controller of the *May* reference, or to combine the teachings of the two references.

For these reasons, independent Claim 1 recites unique and non-obvious limitations that are not disclosed, suggested or even hinted at in the *Agrawal* reference, the *May* reference, the *Gulliford* reference, and the *Burt* reference, or in any combination of two or more of the *Agrawal*, *May*, *Gulliford* and *Burt* references. This being the case, Claim 1 is patentable over the cited prior art references. Also, amended independent Claims 9 and 17 recite limitations that are analogous to the unique and non-obvious limitations recited in independent Claim 1. This being the case, independent Claims 9 and 17 also are patentable over the *Agrawal* reference, the *May* reference, the *Gulliford* reference, and the *Burt* reference, or any combination thereof.

Finally, dependent Claims 2 and 4-8, which depend from independent Claim 1, dependent Claims 10 and 12-16, which depend from Claim 9, and dependent Claims 18-20, which depend from

Claim 17, contain all of the unique and non-obvious limitation of their respective base claims. This being the case, Claims 2, 4-8, 10, 12-16 and 18-20 are patentable over the *Agrawal* reference, the *May* reference, the *Gulliford* reference, and the *Burt* reference, or in any combination of two or more of the *Agrawal*, *May*, *Gulliford* and *Burt* references.

The Applicant also disagrees with the Examiner's rejections of Claims 2, 4-10 and 12-20 based on additional misdescriptions and/or misapplications of the *Agrawal*, *May*, *Gulliford* and *Burt* references to at least some of Claims 2, 4-10 and 12-20. However, the Applicant's arguments regarding those other shortcomings of the *Agrawal*, *May*, *Gulliford* and *Burt* references are moot in view of the Claim 1 arguments above. However, the Applicant reserves the right to dispute in future Office Action responses the appropriateness and the applications of the *Agrawal*, *May*, *Gulliford* and *Burt* references to the claims of the present application, including the right to dispute assertions made by the Examiner in the July 18, 2005, final Office Action.

SUMMARY

For the reasons given above, the Applicant respectfully requests reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *jmockler@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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John T. Mockler
Registration No. 39,775

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *jmockler@davismunck.com*